L	Hits	Search Text	DB	Time stamp
Number				-
37	449	(thin adj film adj transistor) and (gate	USPAT;	2004/12/02
		adj line) and (data adj line) and pad and	US-PGPUB	17:00
		(contact adj hole)		
38	224		USPAT;	2004/12/02
		adj line) and (data adj line) and pad and	US-PGPUB	16:36
		(contact adj hole)) and @ad<20020417		
41	4	(((thin adj film adj transistor) and	USPAT;	2004/12/02
		(gate adj line) and (data adj line) and	US-PGPUB	17:00
		pad and (contact adj hole)) and		
		@ad<20020417) and (data adj link)		
42	224	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	USPAT;	2004/12/02
		adj line) and (data adj line) and pad and	US-PGPUB	16:38
		(contact adj hole)) and @ad<20020417		
43	42	,	EPO; JPO;	2004/12/02
		adj line) and (data adj line) and pad and	DERWENT;	17:01
		(contact adj hole)	IBM_TDB	

US-PAT-NO: 6300152

DOCUMENT-IDENTIFIER: US 6300152 B1

TITLE: Method for manufacturing a panel for

a liquid crystal

display with a plasma-treated organic

insulating layer

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Brief Summary Text - BSTX (17):

Data pads connected to ends of the data lines may be formed. A data <u>pad</u> is exposed through a contact hole of the organic insulating layer. The data pads are preferably treated by argon sputtering along with the drain electrodes. A redundant data <u>pad</u> of the transparent conducting layer may be formed to contact with a data <u>pad</u>.

Brief Summary Text - BSTX (20):

Color filters may be formed on a thin film transistor array panel. At this time, the color filters are patterned to form contact holes exposing the drain electrodes. The color filters and the contact holes are treated by plasma to remove residue and to increase surface roughness. Then, a transparent conducting layer is deposited on the color filters.

Drawing Description Text - DRTX (2):
FIGS. 1, 3, and 6 are layout views of a substrate in steps of manufacturing
an amorphous silicon thin film transistor array panel according to a first embodiment of the present invention.

Drawing Description Text - DRTX (6):

FIGS. 9 and 10 are a cross-sectional views showing a process of treating an organic insulating layer in the manufacturing process of an amorphous silicon thin film transistor array panel according to a second embodiment.

Drawing Description Text - DRTX (7):

FIG. 11 is a cross-sectional view showing a process of forming a contact hole in the manufacturing process of an amorphous silicon thin film transistor array panel according to a third embodiment.

Drawing Description Text - DRTX (8):
FIG. 12 is a cross-sectional view of an amorphous silicon thin film
transistor array panel according to a fourth embodiment.

Detailed Description Text - DETX (3):

FIGS. 1 to 8 are layout views and cross-sectional views of a substrate in the steps of manufacturing an amorphous silicon thin film transistor array panel according to a first embodiment of the present invention.

Detailed Description Text - DETX (4):

As shown in FIGS. 1 and 2, a metal layer is deposited on an insulating substrate 10 and patterned to form a gate wire. The gate wire includes a plurality of gate lines 100 extending in a horizontal direction on FIG. 1, a plurality of gate electrodes 110 connected to the gate line 100, and a plurality of gate pads 120 connected to an end of the gate line 100 and receiving scanning signals.

Detailed Description Text - DETX (6):
Another metal layer of chromium (Cr), molybdenum (Mo),

and molybdenum alloy

(Mo-alloy) is deposited on the semiconductor layer 200, the ohmic contact layer

210, and the gate insulating layer 20 and then patterned to form a data wire.

The data wire includes a plurality of data lines 300 extending in a vertical

direction on FIG. 1, a plurality of source electrodes 310 connected to the data

<u>line</u> 300 and overlapping a side portion of the semiconductor layer 200, a

plurality of drain electrodes 320 overlapping another side portion of the

semiconductor layer 200 at the opposite side of the source electrode 310, and a

plurality of data pads 330 connected to an end of the $\underline{\text{data}}$ line 300.

Detailed Description Text - DETX (8):

As shown in FIGS. 3 and 4, the organic insulating layer 30 is illuminated

and developed to form contact holes C1, C2, and C3 respectively exposing the

drain electrode 320, the gate insulating layer 20 on the gate pad 120 and the

data **pad** 330. The exposed portion of the gate insulating layer 20 is etched to

expose the gate pad 120 through the contact hole C2. At this time, some

residues of the organic insulating layer 30 may remain in the contact holes C1, C2, and C3.

Detailed Description Text - DETX (10):

As shown in FIGS. 6 and 7, a transparent conducting layer such as

indium-tin-oxide (ITO) is deposited on the organic insulating layer 30. A

photoresist layer pattern 40 is formed on the transparent conducting layer.

The transparent conducting layer is etched by using the photoresist layer

pattern 40 as mask to form a pixel electrode 410, a redundant gate pad 420, and

a redundant data pad 430. At this time, the pixel

electrode 410, the redundant gate <u>pad</u> 420, and the redundant data <u>pad</u> 430 are respectively connected to the drain electrode 320, the gate <u>pad</u> 120, and the data <u>pad</u> 330 through the contact holes C1, C2, and C3. The pixel electrode 410 is located in a pixel area surrounded by the gate lines 100 and the data lines 300. Boundaries of the pixel electrode 410 overlap the gate lines 100 and the data lines 300.

Detailed Description Text - DETX (12): As described above, the method of manufacturing an amorphous silicon thin film transistor array panel according to the first embodiment of the present invention that treats the organic insulating layer 30 by argon plasma, reduces the contact resistance between the pixel electrode 410 and the drain electrode 320 because the residues in the contact holes C1, C2, and C3 are removed. The method also improves the adhesion between the ITO layer and the organic insulating layer because of the increased roughness of the organic insulating layer 30. Therefore, the ITO patterns 410, 420, and 430 are prevented from over-etching and undercutting during the wet-etch patterning. As a result, the ITO patterns 410, 420, and 430 may keep uniformity in width.

Detailed Description Text - DETX (14):
FIGS. 9 and 10 are a cross-sectional views showing a process of treating an organic insulating layer in the manufacturing process of an amorphous silicon
thin film transistor array panel according to a second embodiment.

Detailed Description Text - DETX (15):

At first, by the same method as shown in FIGS. 1 to 4, a metal layer is

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deposited on an insulating substrate 10 and patterned to
form a gate wire.
                   The
gate wire includes a plurality of gate lines 100 extending
in a horizontal
direction on FIGS. 1 and 3, a plurality of gate electrodes
110 connected to the
gate line 100, and a plurality of gate pads 120 connected
to each end of the
gate lines 100 and receiving scanning signals. Next, a
gate insulating layer
20, an amorphous silicon layer and a doped amorphous
silicon layer are
sequentially deposited on the gate wire 100,110, and 120.
The doped amorphous
silicon layer and the amorphous silicon layer are patterned
at the same time to
form a semiconductor layer 200 and an ohmic contact layer
210 of the gate
electrode 110. Another metal layer is deposited on the
semiconductor layer
200, the ohmic contact layer 210, and the gate insulating
layer 20 and then
patterned to form a data wire. The data wire includes a
plurality of data
lines 300 extending perpendicularly to the gate lines, a
plurality of source
electrodes 310 connected to the data line 300 and
overlapping a side portion of
the semiconductor layer 200, a plurality of drain
electrodes 320 overlapping
another side portion of the semiconductor layer 200 at the
opposite side of the
source electrode 310, and a plurality of data pads 330
connected to each end of
the data lines 300. Next, the portion of the ohmic contact
layer 210 not
covered by the source electrode 310 and the drain electrode
320 is removed. A
photosensitive organic insulating layer 30 is coated
thereon. The organic
insulating layer 30 is irradiated and developed to form
contact holes C1, C2,
and C3 respectively exposing the drain electrode 320, the
gate insulating layer
20 on the gate pad 120, and the data pad 330. The exposed
portion of the gate
insulating layer 20 through the contact hole C2 is etched
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to expose the 'gate

Detailed Description Text - DETX (18):

Afterward, as described in the first embodiment, a pixel electrode 410, a

redundant gate **pad** 420, and the redundant data **pad** 430 are formed.

Detailed Description Text - DETX (22):

FIG. 11 is a cross-sectional view showing a process of forming contact holes $% \left(1\right) =\left(1\right) +\left(1\right$

in the manufacturing process of an amorphous silicon thintenses than transistor array

panel according to a third embodiment.

Detailed Description Text - DETX (25):

Therefore, an increase of contact resistance between the drain electrode $320\,$

and the pixel electrode 410 and between the data \underline{pad} 330 and the redundant data

pad 430 by the chromium oxide layer 31 is prevented.

Detailed Description Text - DETX (26):

In the above description, thin film transistor array panels using amorphous silicon as a semiconductor layer have been described. However, the present invention can be applied to a thin film transistor array panels using

Detailed Description Text - DETX (27):

polysilicon as a semiconductor layer.

FIG. 12 is a cross-sectional view of an amorphous silicon $\underline{\text{thin film}}$

transistor array panel according to a fourth embodiment.

Detailed Description Text - DETX (33):

The methods of manufacturing $\underline{\text{thin film transistor}}$ array panels according to

the first embodiment through the fourth embodiment may be applied to

manufacturing a color filter array panel using an organic insulating layer as a passivation layer. Particularly, this method is essential in manufacturing a color filter array panel for a patterned vertically aligned (PVA) mode LCD that requires a transparent electrode to be patterned.

Detailed Description Text - DETX (44):

Next, a sixth and seventh embodiment having a color filter structure on a thin film transistor (TFT) array panel will be described.

Detailed Description Text - DETX (47):

A semiconductor layer 220 of amorphous silicon is formed on the gate insulating layer and above the gate electrode 130. An

ohmic contact layer 230 of doped amorphous silicon is formed on the semiconductor layer 220. This

ohmic contact layer 230 is separated into two portions. A data wire including

a plurality of data lines (not illustrated) and source and drain electrodes 340

and 350 contacting with the ohmic contact layer 230, etc. are formed on the

gate insulating layer 20. At this point, the $\underline{\text{data line}}$ may be about 20 .mu.m

wide, which is much wider than the conventional device that is $6 \, .mu.m$ to $7 \,$

.mu.m. This is possible because color filters 60 are formed on the thin film transistor array panel.

Detailed Description Text - DETX (53):

Next, a conducting layer of an inert metal such as $\operatorname{chromium}$ and $\operatorname{molybdenum}$

is deposited and patterned to form a data wire including a data line (not

illustrated) and a source electrode and a drain electrode. The exposed portion

of the ohmic contact layer 230 between the source electrode 340 and the drain $\frac{1}{2}$

electrode 350 is removed by etching.